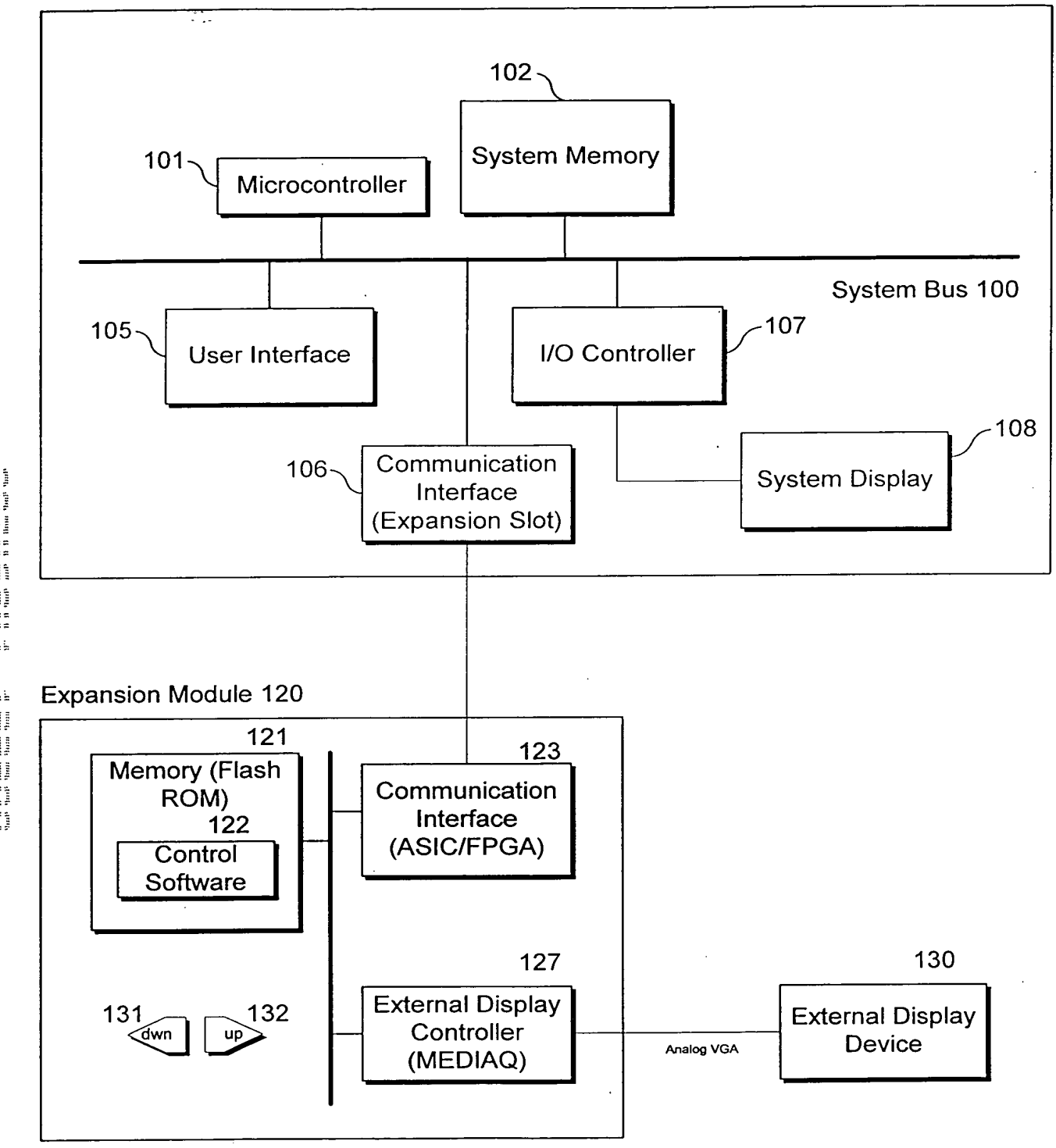

Handheld Computing System 110
102
System Memory
101
Microcontroller
System Bus 100
105
User Interface
I/O Controller
107
108
System Display
106
Communication Interface (Expansion Slot)
Expansion Module 120
121
Memory (Flash ROM)
122
Control Software
123
Communication Interface (ASIC/FPGA)
127
External Display Controller (MEDIAQ)
130
External Display Device
131
dwn
132
up
Analog VGA

FIG. 1

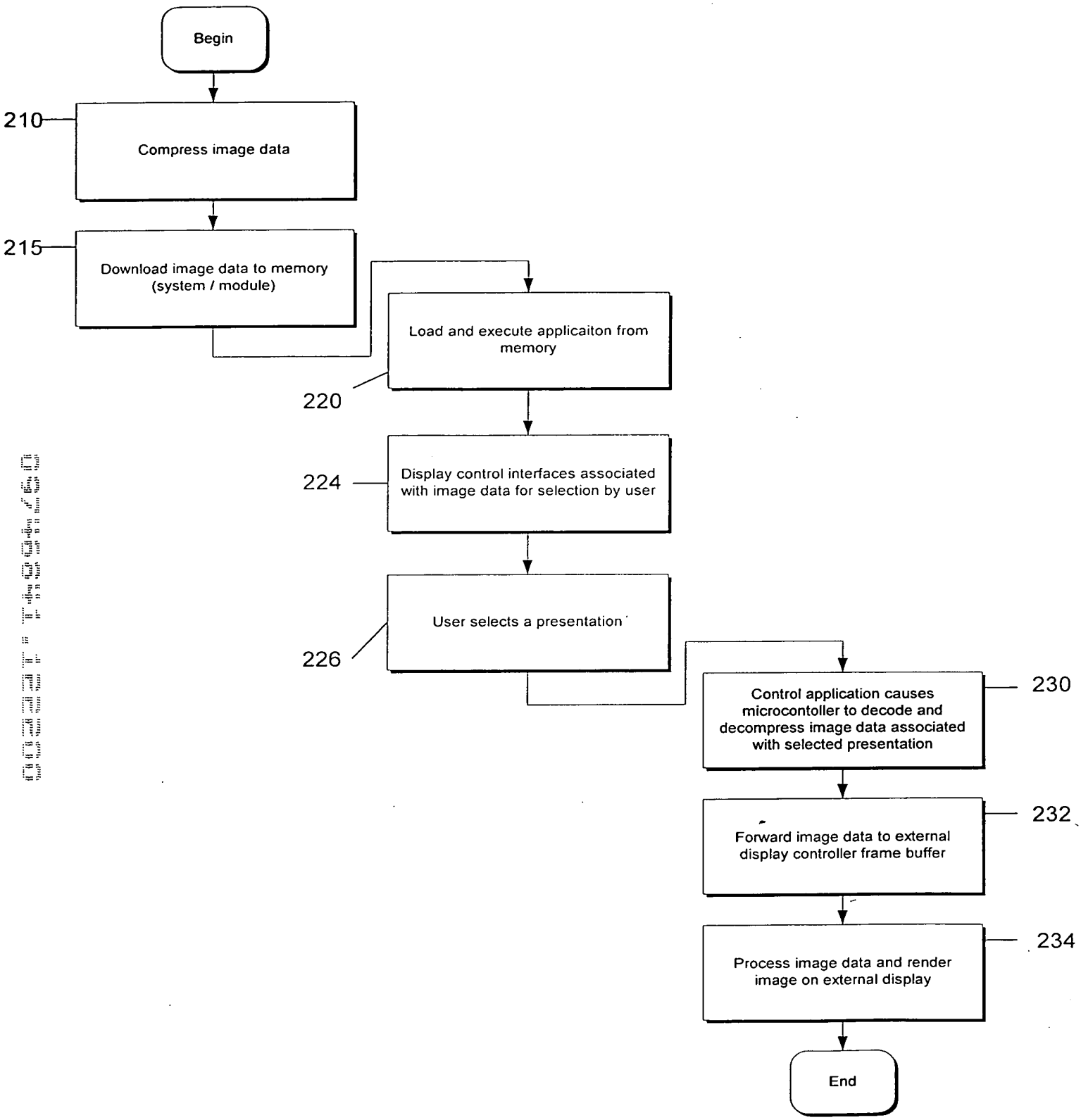

Begin
210
Compress image data
215
Download image data to memory (system / module)
Load and execute applicaiton from memory
220
224
Display control interfaces associated with image data for selection by user
User selects a presentation
226
230
Control application causes microcontoller to decode and decompress image data associated with selected presentation
232
Forward image data to external display controller frame buffer
234
Process image data and render image on external display
End

FIG. 2

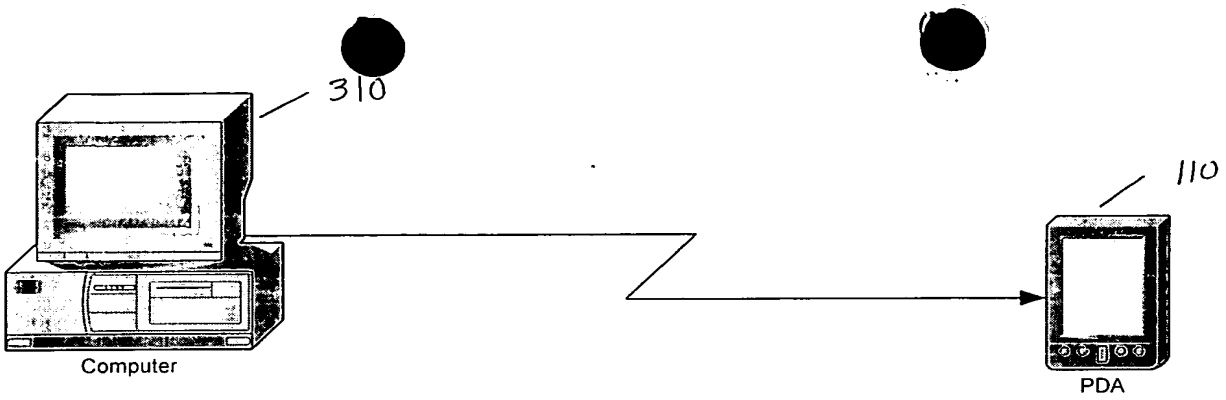


FIG. 3A

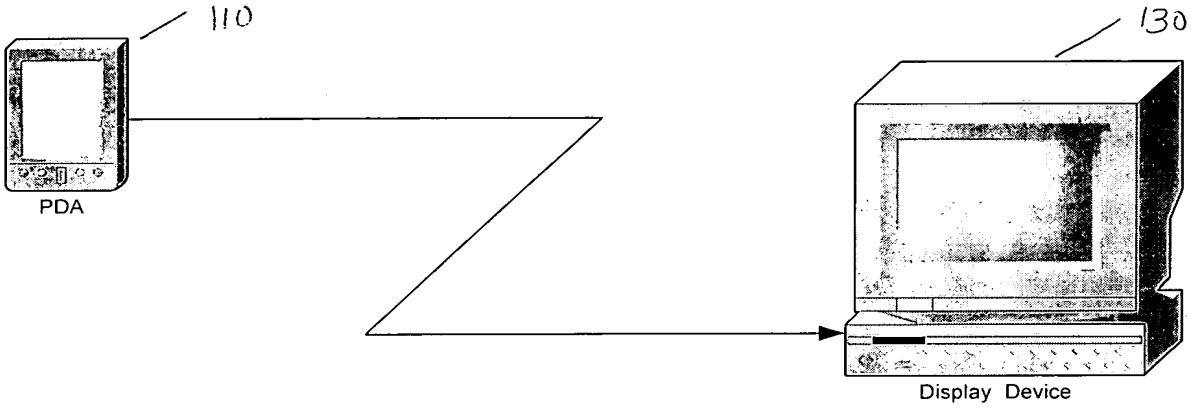


FIG. 3B

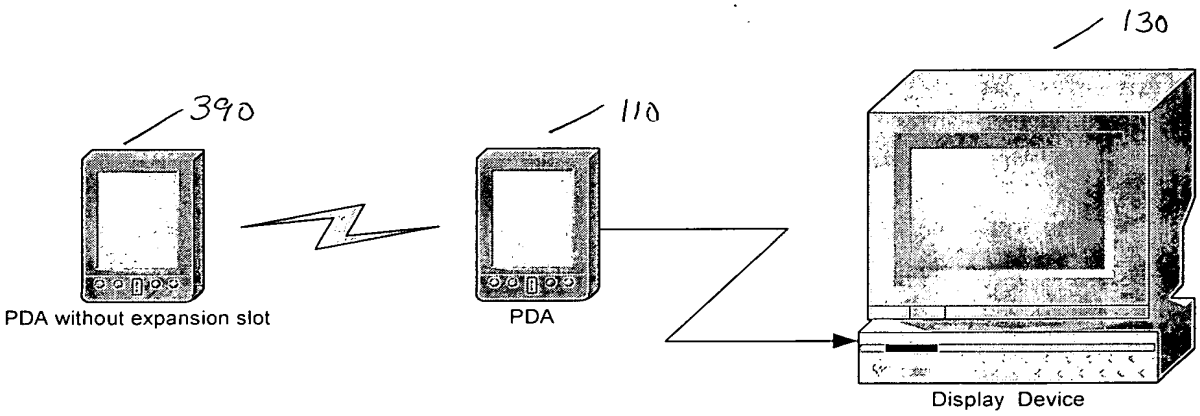


FIG. 3C

Menu: FILE

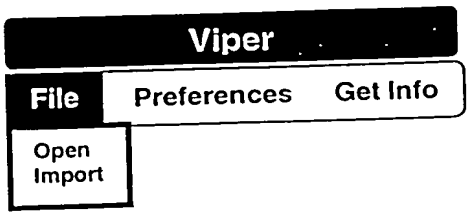


FIG. 4A

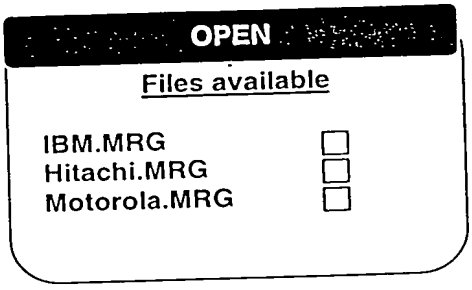


FIG. 4B

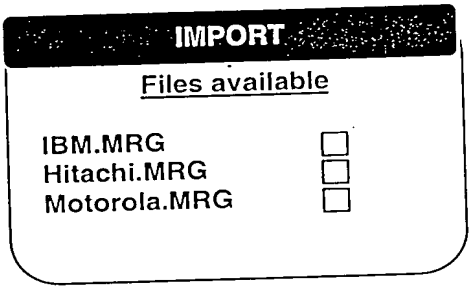


FIG. 4C

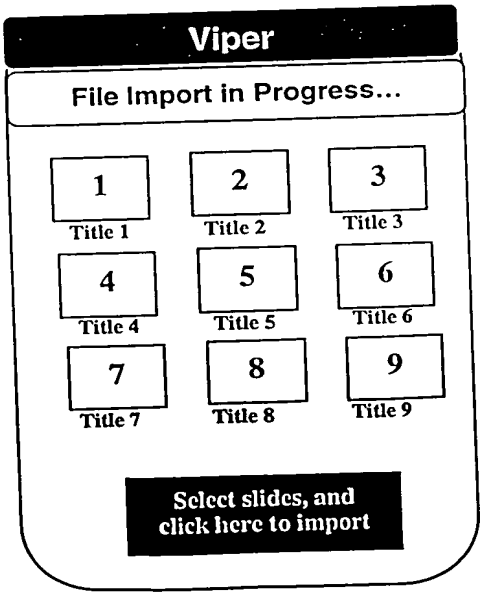


FIG. 4D

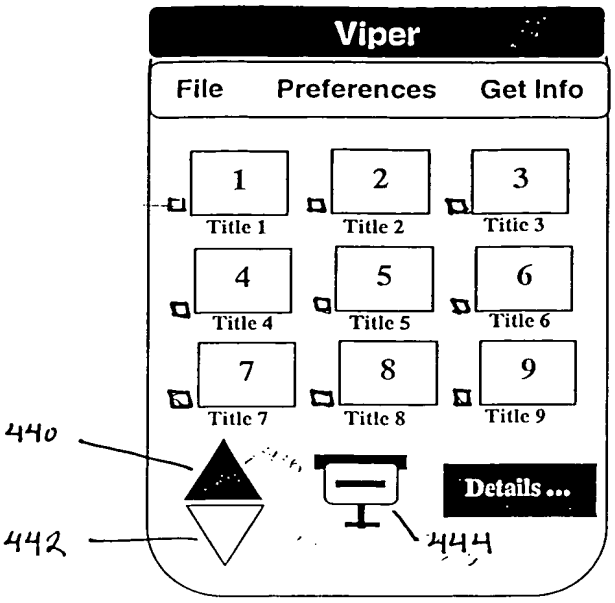


FIG. 4E

Move the selected slide up

Move the selected slide down

Start Slide Show

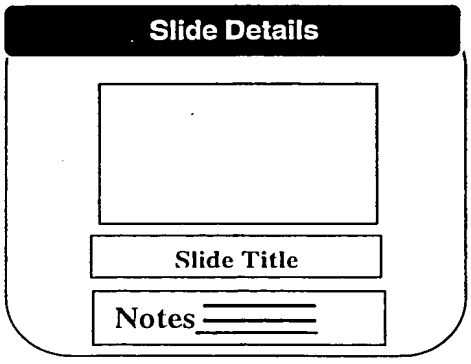


FIG. 4F

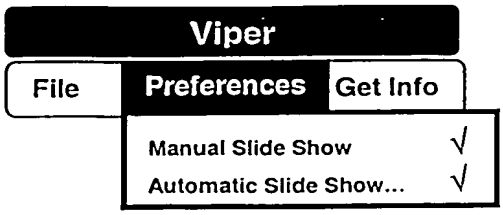


FIG. 4G

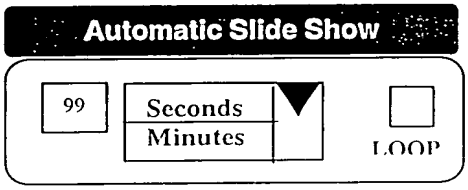


FIG. 4H

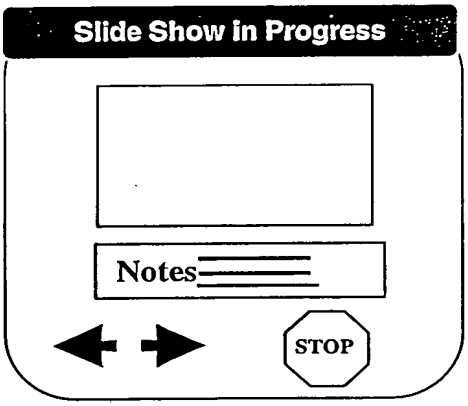


FIG. 4I

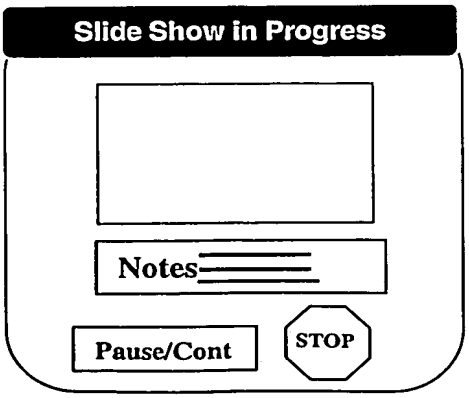


FIG. 4J

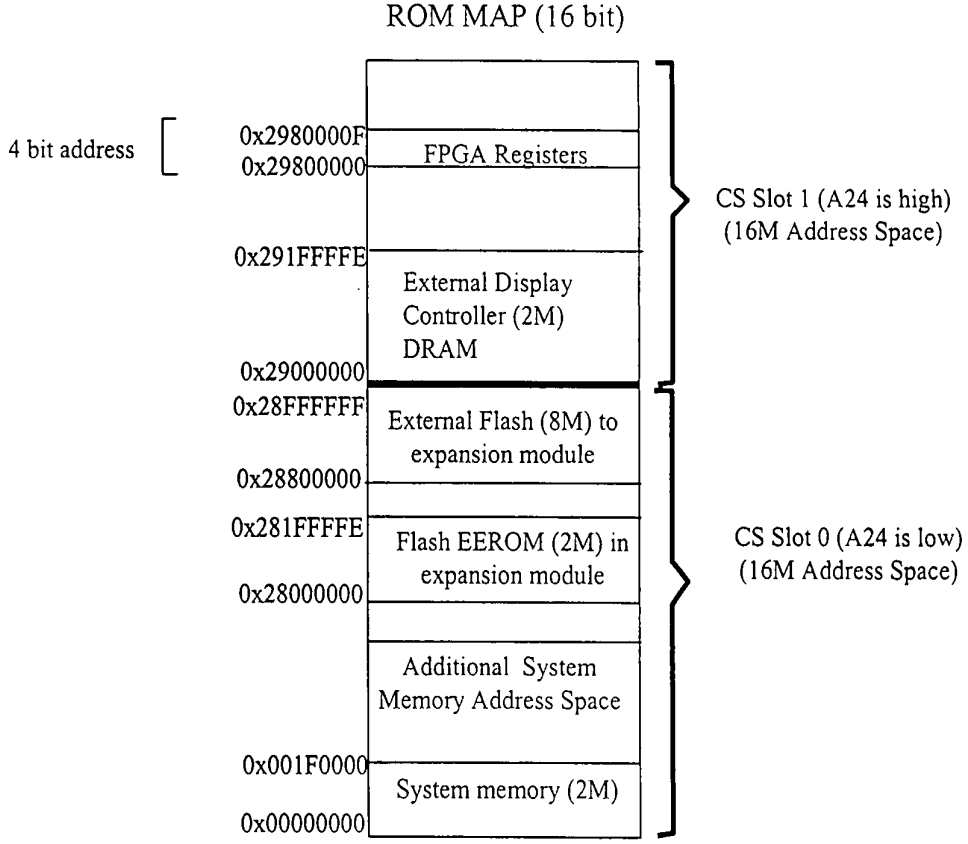

ROM MAP (16 bit)
4 bit address
0x2980000F
0x29800000
FPGA Registers
0x291FFFFE
External Display Controller (2M) DRAM
0x29000000
CS Slot 1 (A24 is high) (16M Address Space)
0x28FFFFFF
External Flash (8M) to expansion module
0x28800000
0x281FFFFE
Flash EEROM (2M) in expansion module
0x28000000
Additional System Memory Address Space
0x001F0000
System memory (2M)
0x00000000
CS Slot 0 (A24 is low) (16M Address Space)

Figure 5A

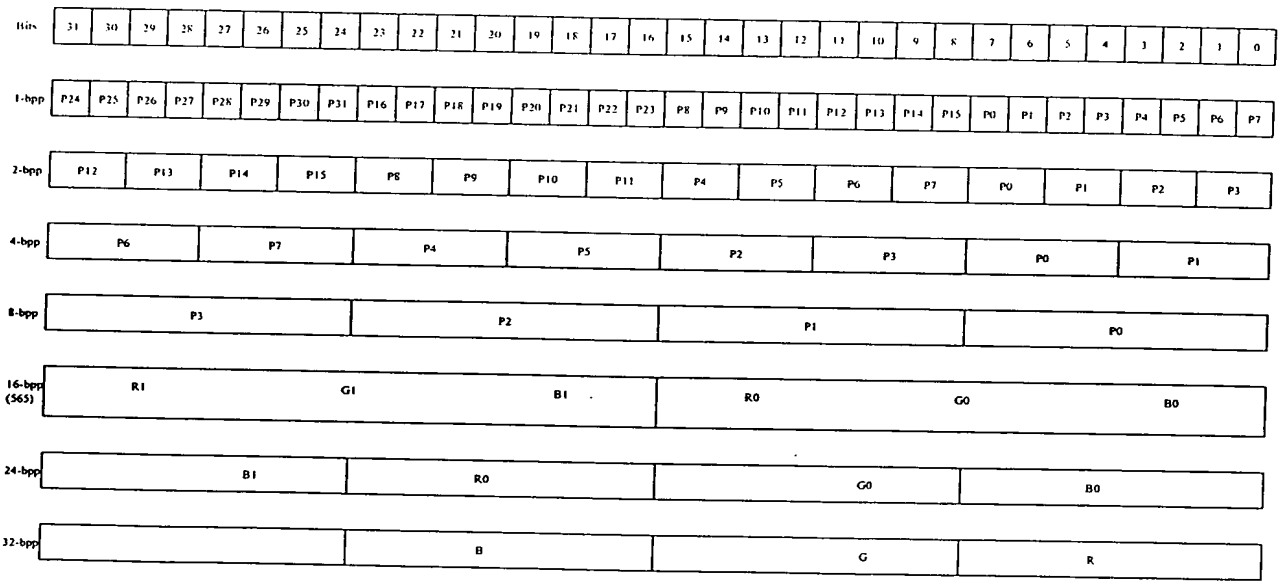

Bits
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
1-bpp
P24 P25 P26 P27 P28 P29 P30 P31 P16 P17 P18 P19 P20 P21 P22 P23 P8 P9 P10 P11 P12 P13 P14 P15 P0 P1 P2 P3 P4 P5 P6 P7
2-bpp
P12 P13 P14 P15 P8 P9 P10 P11 P4 P5 P6 P7 P0 P1 P2 P3
4-bpp
P6 P7 P4 P5 P2 P3 P0 P1
8-bpp
P3 P2 P1 P0
16-bpp (565)
R1 G1 B1 R0 G0 B0
24-bpp
B1 R0 G0 B0
32-bpp
B G R

FIG. 5B

Register Addresses		Read (16 bits)	Write (16 bits)
High Address bits	Low Address (0-7)		
0x298000	00	ID, Version #, Status	Interrupt, Timer, Control
0x298000	02	Microcontroller Data Exchange Register	Microcontroller Data Exchange Register
0x298000	04	Microcontroller Data Transfer Status Register	Microcontroller Data Transfer Status Register
0x298000	06-0f	Reserved for Future	Reserved for Future

FIG. 5C

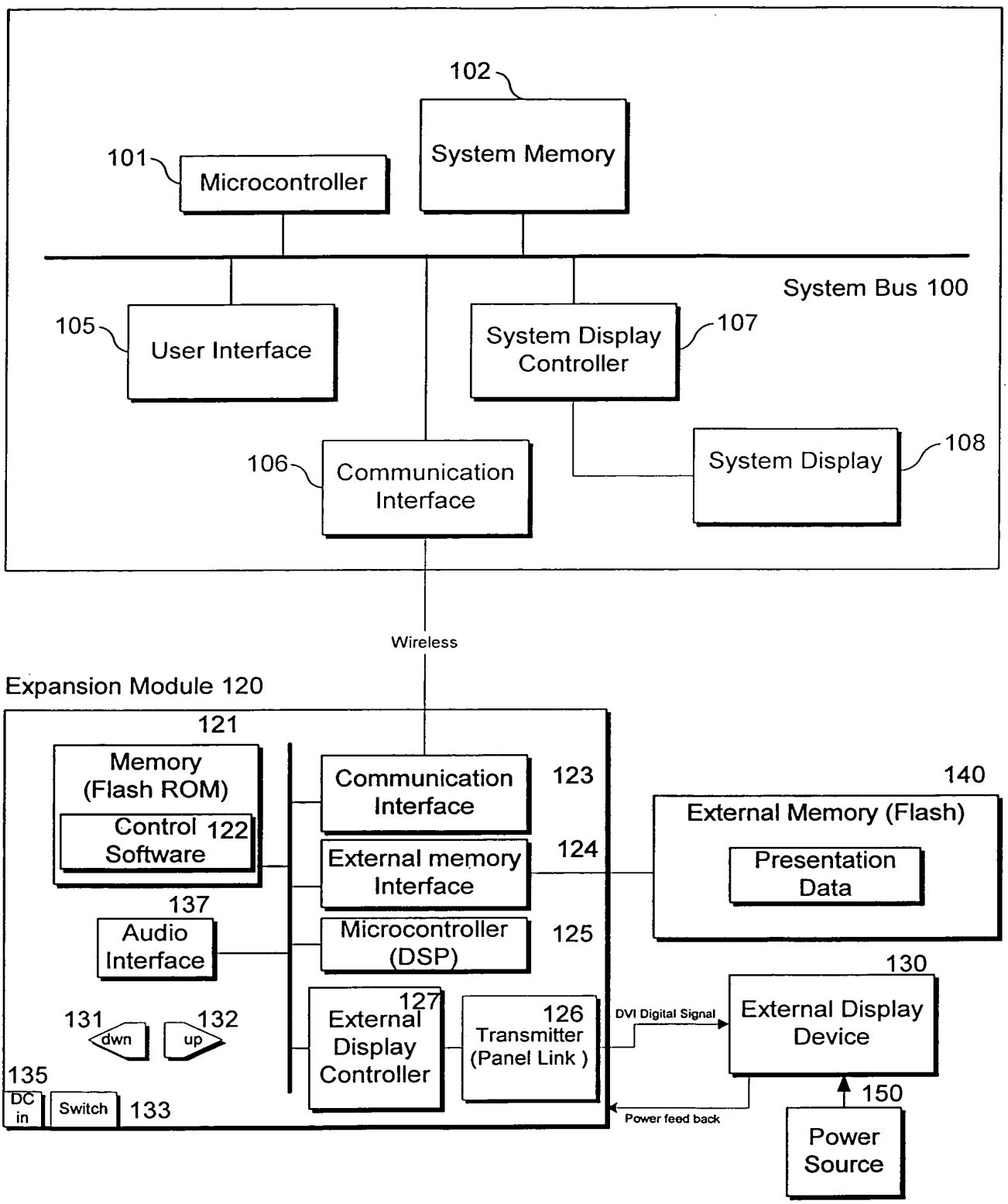
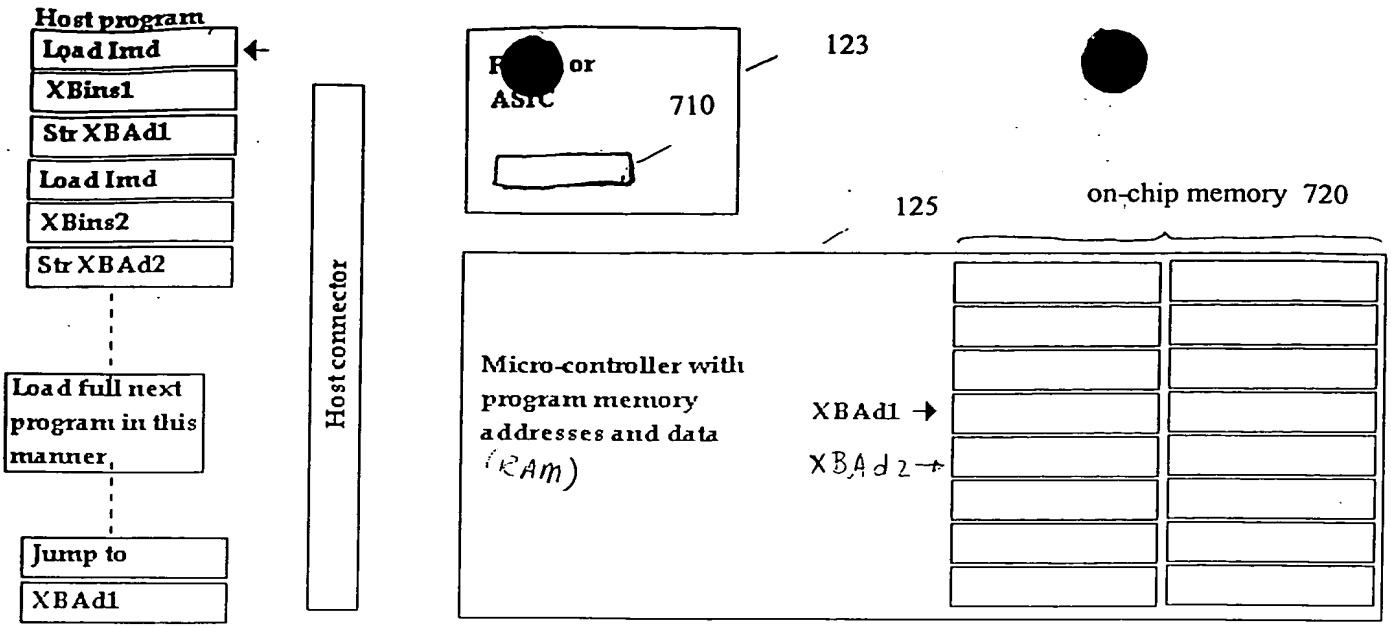

Handheld Computing System 110
102
System Memory
101
Microcontroller
System Bus 100
105
User Interface
System Display Controller
107
106
Communication Interface
System Display
108
Wireless
Expansion Module 120
121
Memory (Flash ROM)
Control Software
122
Communication Interface
123
140
External Memory (Flash)
Presentation Data
External memory Interface
124
137
Audio Interface
Microcontroller (DSP)
125
130
131
dwn
132
up
127
External Display Controller
126
Transmitter (Panel Link)
DVI Digital Signal
External Display Device
135
DC in
Switch
133
Power feed back
150
Power Source

FIG. 6



After reset

FIG. 7A

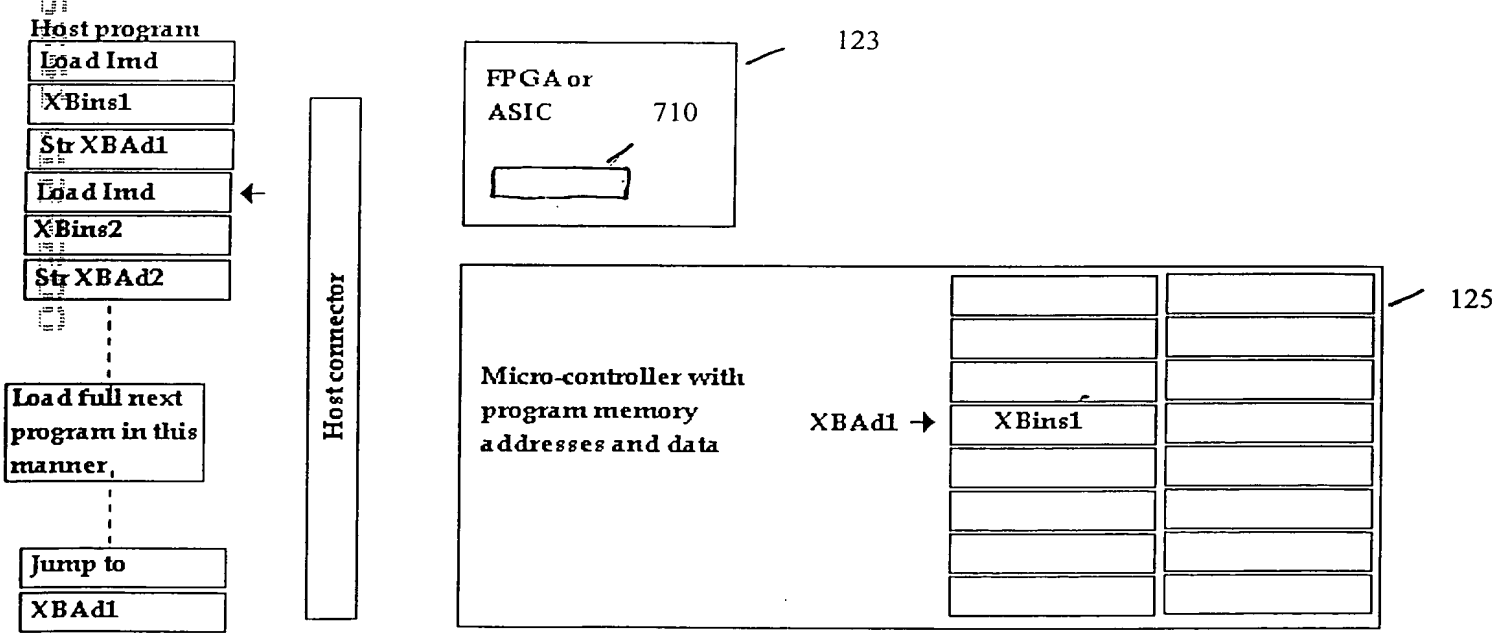


FIG. 7B

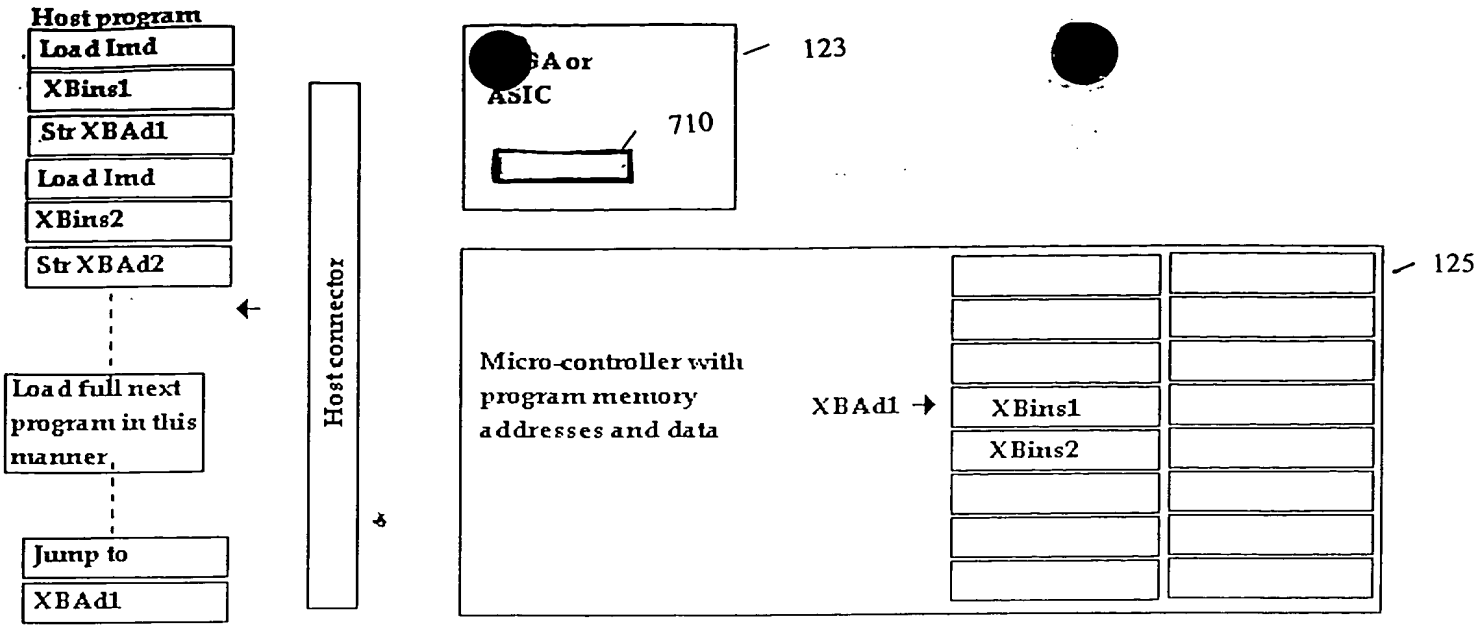

Host program
Load Imd
XBins1
Str XBAd1
Load Imd
XBins2
Str XBAd2
Load full next program in this manner
Jump to
XBAd1
Host connector
ASIC
710
123
Micro-controller with program memory addresses and data
XBAd1
XBins1
XBins2
125

FIG. 7C

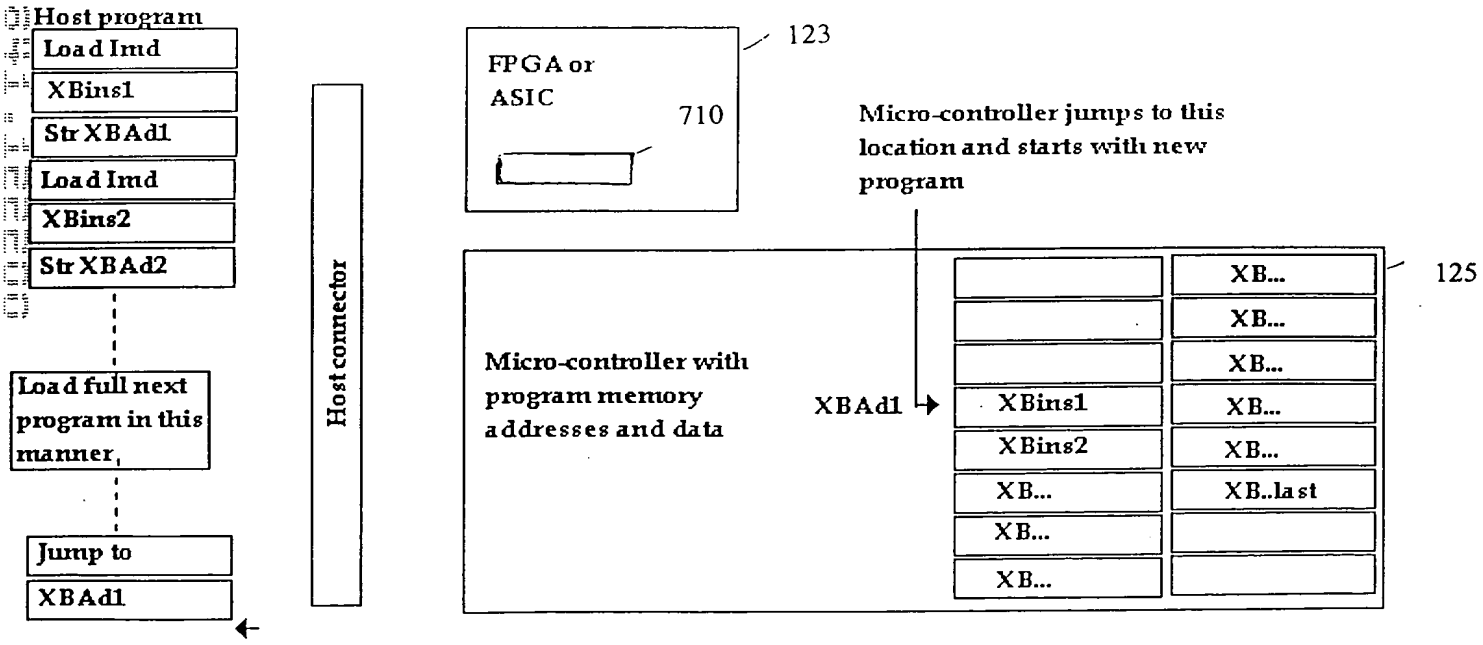

Host program
Load Imd
XBins1
Str XBAd1
Load Imd
XBins2
Str XBAd2
Load full next program in this manner
Jump to
XBAd1
Host connector
FPGA or
ASIC
710
123
Micro-controller jumps to this location and starts with new program
Micro-controller with program memory addresses and data
XBAd1
XBins1
XBins2
XB...
XB..last
125

FIG. 7D

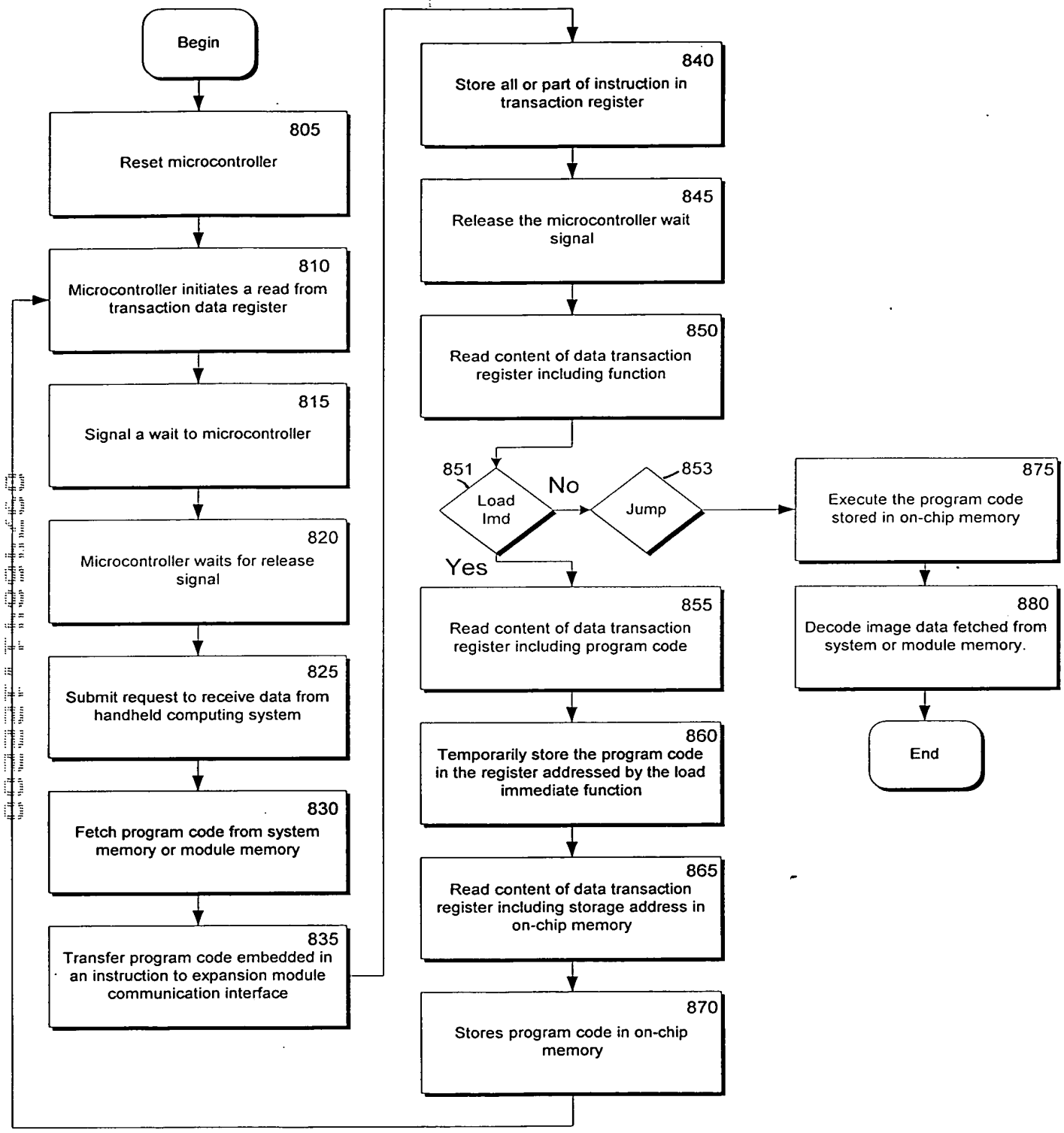

Begin
805
Reset microcontroller
810
Microcontroller initiates a read from transaction data register
815
Signal a wait to microcontroller
820
Microcontroller waits for release signal
825
Submit request to receive data from handheld computing system
830
Fetch program code from system memory or module memory
835
Transfer program code embedded in an instruction to expansion module communication interface
840
Store all or part of instruction in transaction register
845
Release the microcontroller wait signal
850
Read content of data transaction register including function
851
Load Imd
No
853
Jump
Yes
855
Read content of data transaction register including program code
860
Temporarily store the program code in the register addressed by the load immediate function
865
Read content of data transaction register including storage address in on-chip memory
870
Stores program code in on-chip memory
875
Execute the program code stored in on-chip memory
880
Decode image data fetched from system or module memory.
End

FIG. 8

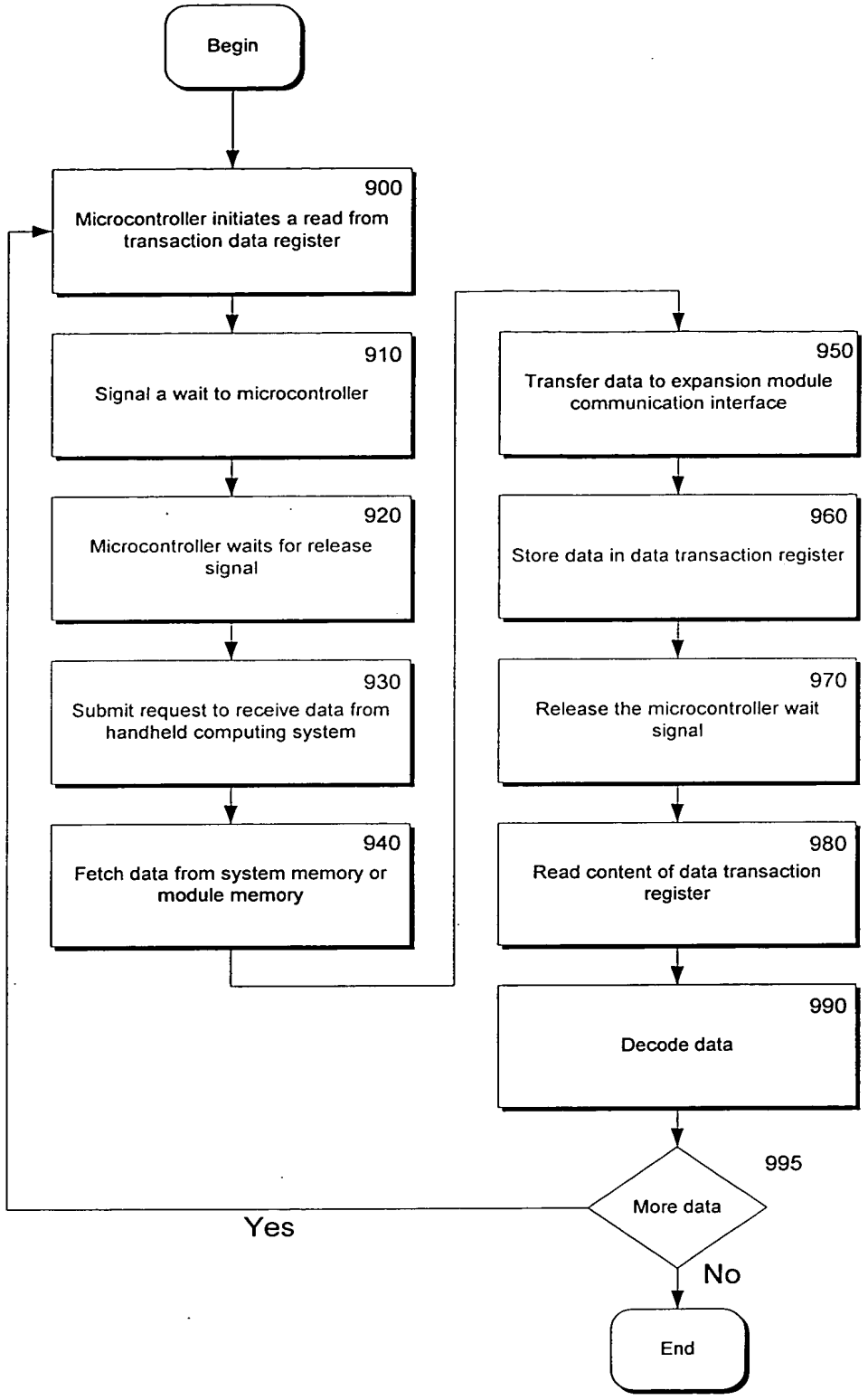

Begin
900
Microcontroller initiates a read from transaction data register
910
Signal a wait to microcontroller
920
Microcontroller waits for release signal
930
Submit request to receive data from handheld computing system
940
Fetch data from system memory or module memory
950
Transfer data to expansion module communication interface
960
Store data in data transaction register
970
Release the microcontroller wait signal
980
Read content of data transaction register
990
Decode data
995
More data
Yes
No
End

FIG. 9